

Vishay Sfernice



SMD Wraparound Ultra Low Value Thin Film Resistors



With extremely low resistance and high power capabilities, these ultra low value resistors are available with solderable or weldable terminations.

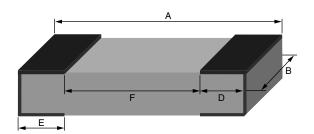
FEATURES

- NiCr + Ta₂O₅ resistive layer
- Pre-soldered or gold terminations
- · No inductance for high frequency applications
- Alumina substrates for high power handling capability
- \bullet Resistance range: 0.1 Ω to 9.99 Ω
- TCR down to 100 ppm/°C
- Power rating: Up to 1 W at + 70 °C



ROHS*
COMPLIANT
GREEN
(5-2008)**

DIMENSIONS in millimeters [inches]



	Α	В									
CASE SIZE	MAX. TOL. + 0.152 (+ 0.006) MIN. TOL. - 0.152 (- 0.006)	MAX. TOL. + 0.127 (+ 0.005) MIN. TOL. - 0.127 (- 0.005)	D/E		F		POWER RATING mW	LIMITING ELEMENT VOLTAGE V	RESISTANCE RANGE (1)		
	NOM.	NOM.	NOM.	TOL.	NOM.	MIN.	MAX.				
0603	1.52 (0.060)	0.85 (0.033)	0.38 (0.015)	0.38	0.76 (0.030)	0.35 (0.014)	1.17 (0.046)	125	50	0.1 Ω to 9.99 Ω	
0705 0805	1.91 (0.075)	1.27 (0.050)			1.15 (0.045)	0.74 (0.029)	1.56 (0.061)	200	50	0.1 Ω to 9.99 Ω	
1206	3.06 (0.120)	1.60 (0.063)	0.40 (0.016)	0.13 (0.005)	2.26 (0.089)	1.85 (0.073)	2.67 (0.105)	330	50	0.1 Ω to 9.99 Ω	
1505	3.81 (0.150)	1.32 (0.052)	0.48 (0.019)	0.48		2.85 (0.112)	2.44 (0.096)	3.26 (0.128)	500	50	0.1 Ω to 9.99 Ω
2010	5.08 (0.200)	2.54 (0.100)		(0.019)	4.12 (0.162)	3.71 (0.146)	4.53 (0.178)	1000	50	0.1 Ω to 9.99 Ω	

Notes

- (1) To be read in conjunction with table "Tolerance and TCR vs. Ohmic Value"
- Size 2512 under development

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply

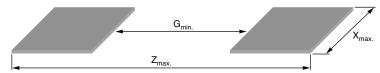
^{**} Please see document "Vishay Material Category Policy": www.vishay.dom/doc?99902

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SUGGESTED LAND PATTERN (to IPC-7351A)



CHIP SIZE	DIMENSIONS (in millimeter)					
CHIP SIZE	Z _{max} .	G _{min.}	X _{max} .			
0603	2.37	0.35	0.98			
0705/0805	2.76	0.74	1.40			
1206	3.91	1.85	1.73			
1505	4.66	2.44	1.45			
2010	5.93	3.71	2.67			

Note

Option: Enlarged Terminations

For stringent and special power dissipation requirements, the thermal resistance between the resistive layer and the solder joint can be reduced using enlarged terminations chip resistors which are soldered on large and thick copper pads acting as heat sinks (see application note:

"Power Dissipation in High Precision Vishay Sfernice Chip Resistors and Arrays (P Thin Film, PRA Arrays, CHP Thick Film)": www.vishay.com/doc?53048).

For enlarged terminations: Please consult Vishay Sfernice.

ELECTRICAL SPECIFICATIONS

Resistance range: 0.1 Ω to 9.99 Ω Resistance tolerance: \pm 1 % to \pm 10 %

Power dissipation: 0.125 mW to 1 W at + 70 °C

Temperature coefficient: Down to 100 ppm/°C

CLIMATIC SPECIFICATIONS

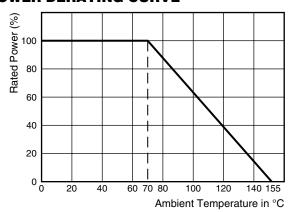
Operating temp. range: - 55 °C to + 155 °C

MECHANICAL SPECIFICATIONS

Substrate:AluminaResistive layer:NiCr + Ta_2O_5 Coating:SiliconeTerminations:Solderable

B type: SnPb over nickel barrier N type: SnAg over nickel barrier G type: Gold over nickel barrier

POWER DERATING CURVE



TOLERANCE AND TCR VS. OHMIC VALUE

VALUE RANGE	TIGHTEST TOLERANCE (%)	BEST TCR (ppm/°C)	TERMINATIONS
0R1 < 0R25	1	300	N or B
0R25 < 0R5	1	200	N or B
0R5 < 9R99	1	100	N or B
0R1 < 0R5	10	300	G
0R5 < 9R99	5	200	G

For technical questions, contact: sfer@vishay.com Document Number: 53018
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[·] Size 2512 under development





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PACKAGING

Several types of packaging are proposed: waffle-pack and tape and reel

	моо	NUMBER OF PIE			
SIZE		WAFFLE PACK 2" × 2"	TAPE A	TAPE WIDTH	
			MIN.	MAX.	
0402					
0603		100			
0805 0705	100	0	100	4000	8 mm
1206		140			
1505		60			
2010				2000	8 mm ⁽¹⁾

Note

- (1) 12 mm on request
- Size 2512 under development

PACKAGING RULES

Waffle Pack

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover.

To get "not stacked up" waffle pack in case of ordered quantity > maximum number of pieces per package: Please concult Vishay/Sfernice for specific ordering code

Tape and Reel

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered is between the MOQ and the maximum reel capacity, only one reel is provided.

When several reels are needed for ordered quantity within MOQ and maximum reel capacity: Please consult Vishay Sfernice for specific ordering code

PERFORMANCE					
		VALUES AND DRIFT			
TESTS	CONDITIONS	MIL-R-55342 REQUIREMENTS	TYPICAL PERFORMANCES		
Thermal shock MIL-R-55342 C MIL-STD-702-Method 1		± 0.25 %	± 0.02 %		
Short time overload	MIL-R-55342 C PARA 3.10.4.7.5	± 0.10 %	± 0.01 %		
Low temperature operation	MIL-R-55342 C PARA 3.9 and 4.7.4	± 0.25 %	± 0.01 %		
Resistance to solder heat	MIL-R-55342 C PARA 3.12, 4.7.7, 4.7.1.2	± 0.25 %	± 0.04 %		
Moisture resistance	MIL-R-55342 C PARA 3.13 and 4.7.8 MIL-STD-202-Method 106	± 0.40 %	± 0.01 %		
High temperature	MIL-R-55342 C PARA 3.11 and 4.7.6	± 0.20 %	± 0.075 %		
MIL-R-55342 C Load life 2000 h Pn at 70 °C MIL-STD-202-Method 108		± 0.50 %	± 0.15 %		

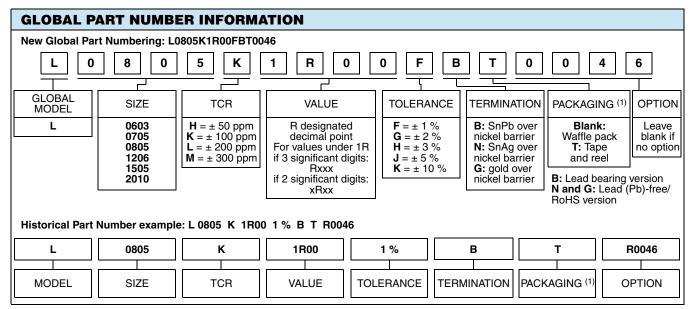
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Note

- (1) For specific quantity of parts per packaging please consult Vishay Sfernice
- Size 2512 under development

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